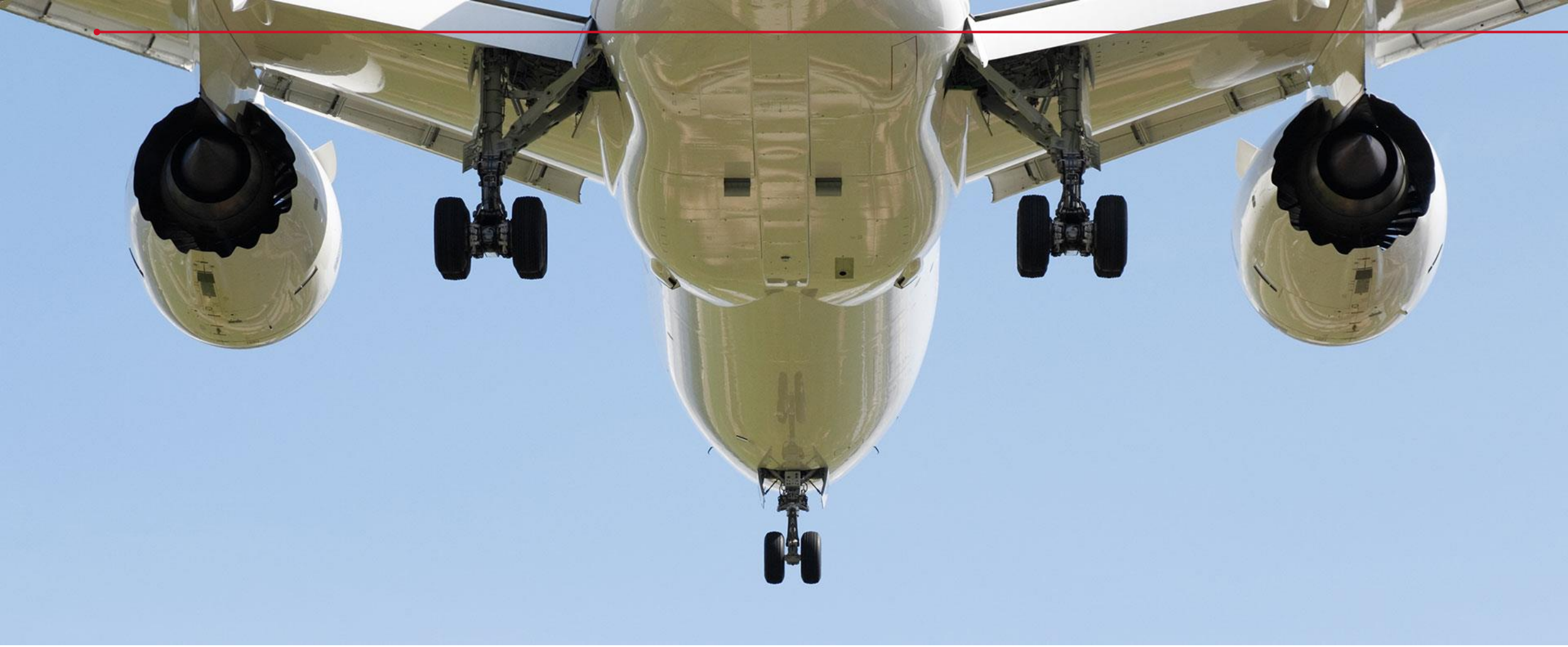

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# MODEL-BASED DESIGN FOR FPGA DEVELOPMENT

GETC-I

# CONTENT

- **Why?**
- **Benefit**
- **Concept**
- **Use case**

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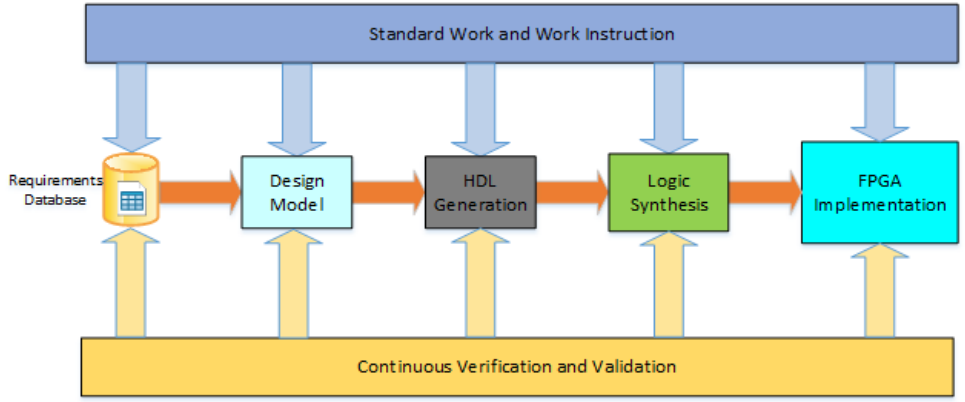
# WHY?

- **Background**
  - In the current projects FW development is done manually without or minimum support of MBD
  - Model based development is the way forward for embedded development as traditional (manual driven) solution require extensive effort.
  - Framework will be used for electronics development for different type of controllers, which are algorithm rich in content.

- **Objectives**
  - A framework and supporting standard work and work instructions for Model based FW algorithm development for aerospace application.
- **KPIs**
  - Reusability for different algorithm module as library
  - Cost reduction (~30 to 40 %)
  - Reduction in lead time for development (~30%)

- **Concept Block Diagram:**




- **Business Impact:**
  - Cost Reduction
    - Rapid initial design (rapid prototyping, continuous validation & verification across the different layer of design)
    - Easy rework and verification (verification based on model, possibility to generate test benches from Models)
  - Reduce risk of design error
  - Lower needed skill level for FPGA design of complex algorithm

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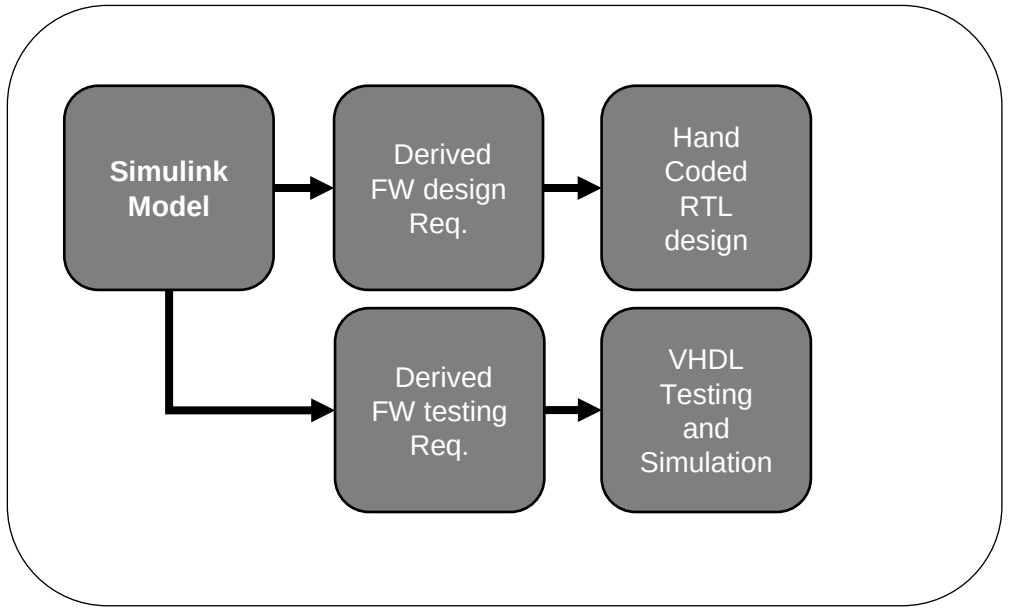
# METHOD DESCRIPTION

## Current State

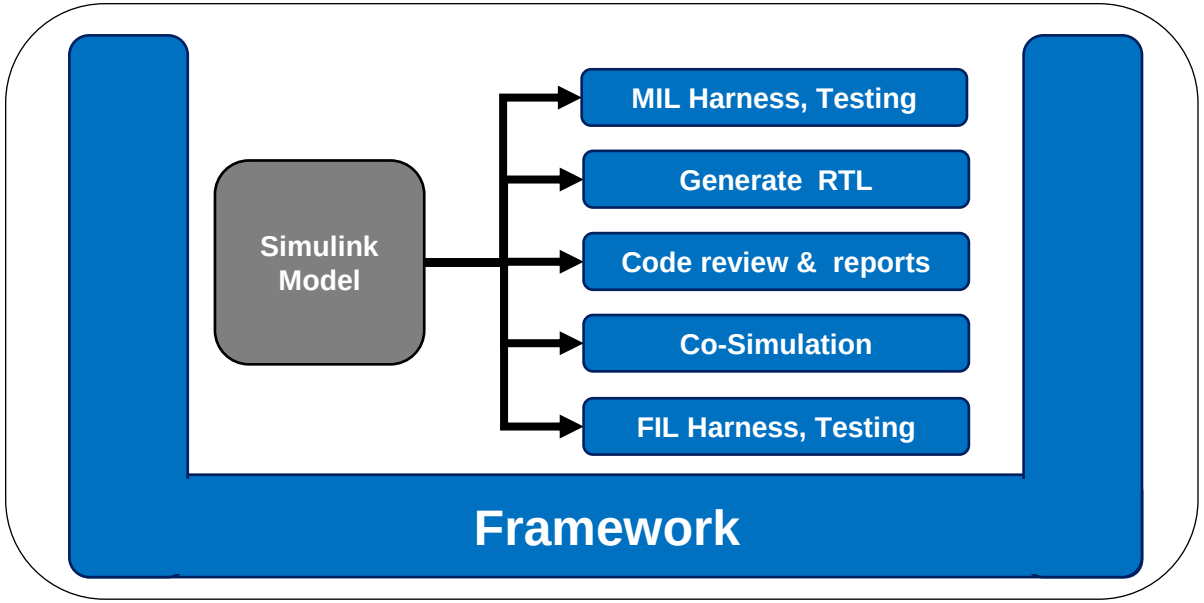



**Challenges:**

- Fixed point algorithm development and verification increase complexity
- Requirements to code generation add multilayer process and risk for error
- Close loop simulation and test analysis not easy in the current FPGA development setup

# METHOD DESCRIPTION

## Future State




## Advantages:

- Reduce time and cost for development
- Early validation and verification using MIL and Co-Simulation (virtual integration)
- Recuse of same test case and plant model for testing
- Reusability and scalability
- Robustness

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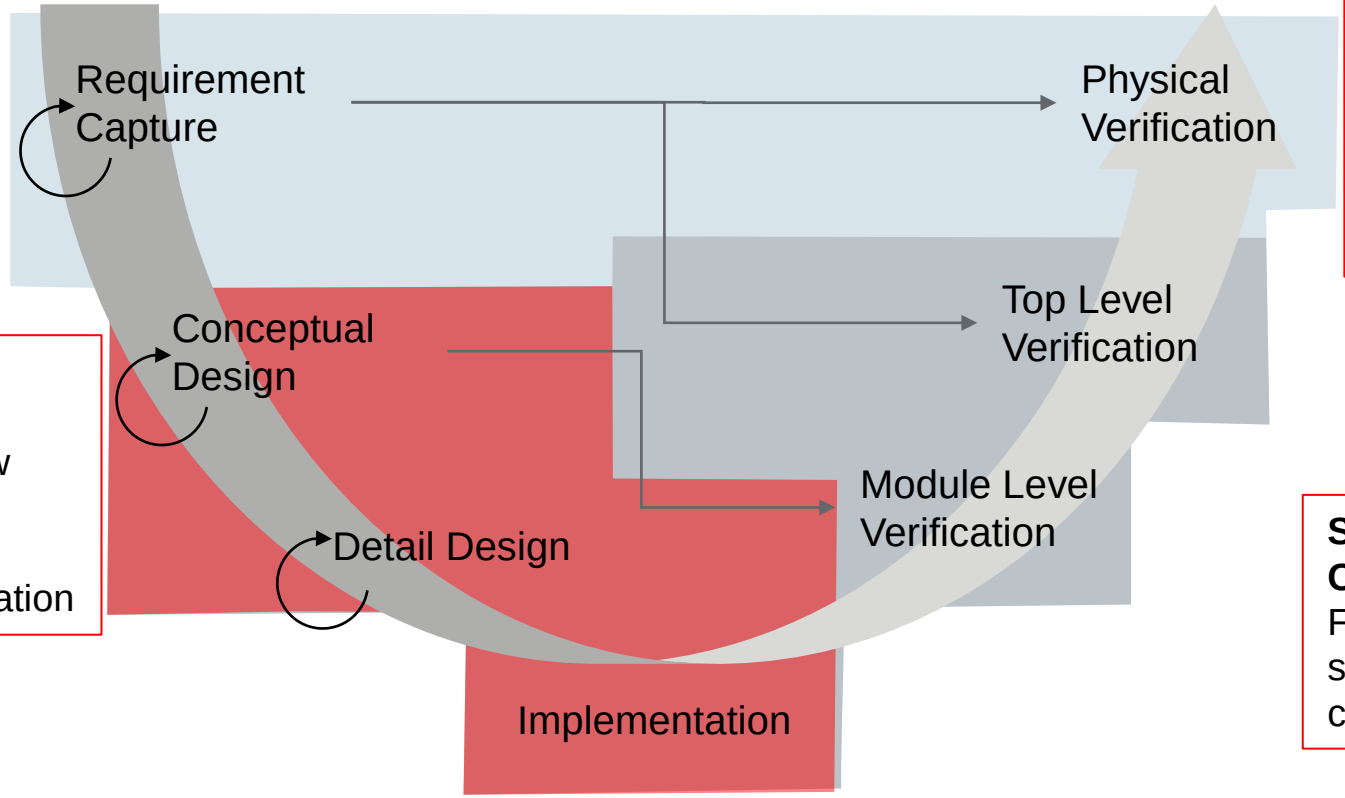
# MBD FOR FW AS PER DO 254: MBD IMPLEMENTATION APPROACH




**First step**
**Design by Model:**
Design Model including Low Level Requirements and Architecture
Automatic HDL code generation

**Third step**
**High Level Modeling & FPGA In the Loop:**
Second step + Specification Model including Functional behavior, interface, performance and safety Verification up to Physical with FIL*

**Second step**
**Co-simulation:**
First step+VHDL simulation result comparison with Model

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# USE CASE

## Motor Control law development:

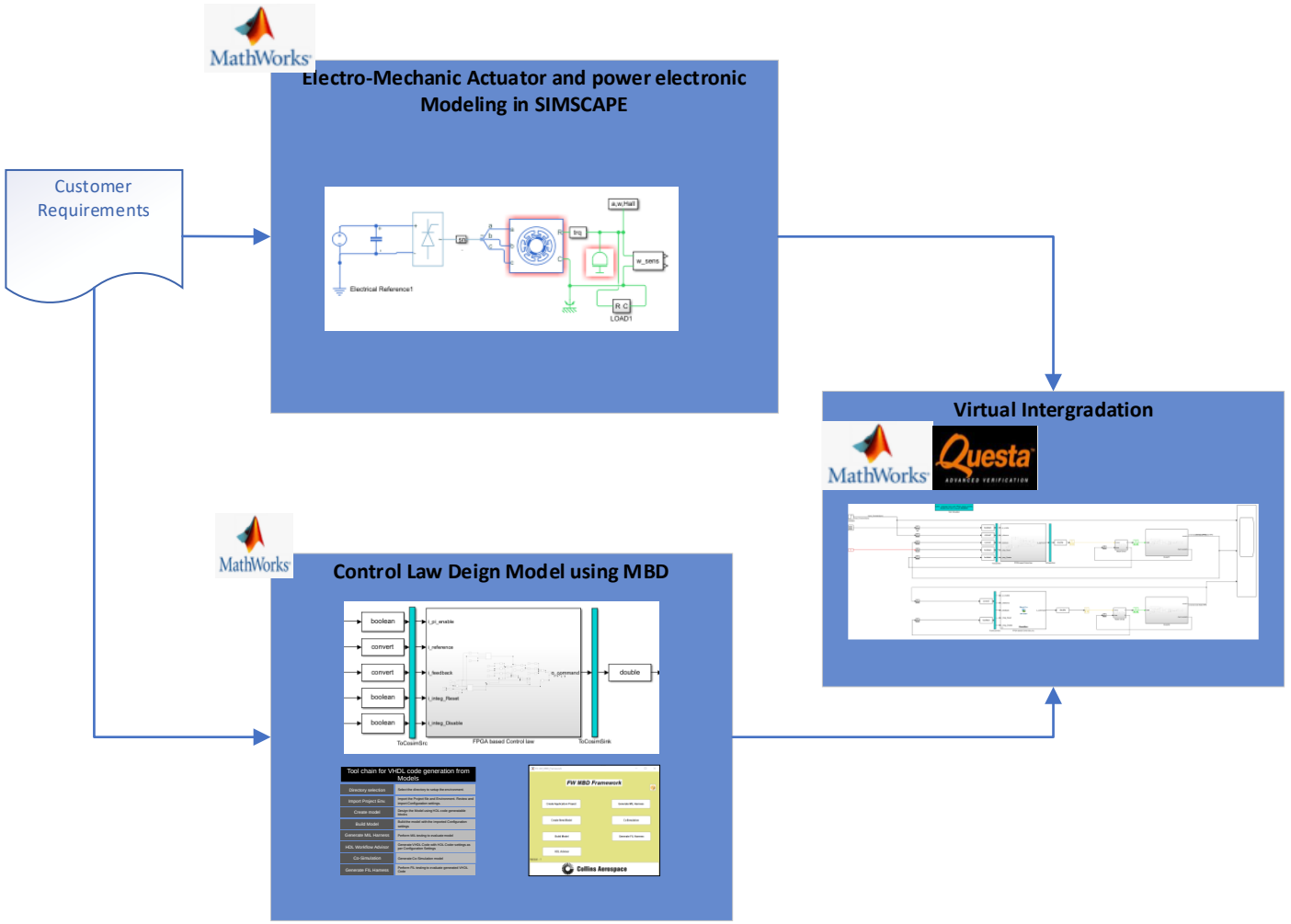
- A multi-Domain problem
  - Embedded system: Control law, sensor processing and BIT (algorithm and signal processing)
  - Physical modeling (Elector-mechanical and sensor modeling)
  - Power electronics modeling (motor derives)

- Flow of information and data from system spec till design

- Design and auto code generation

- Early verification and validation

- Co-Simulation

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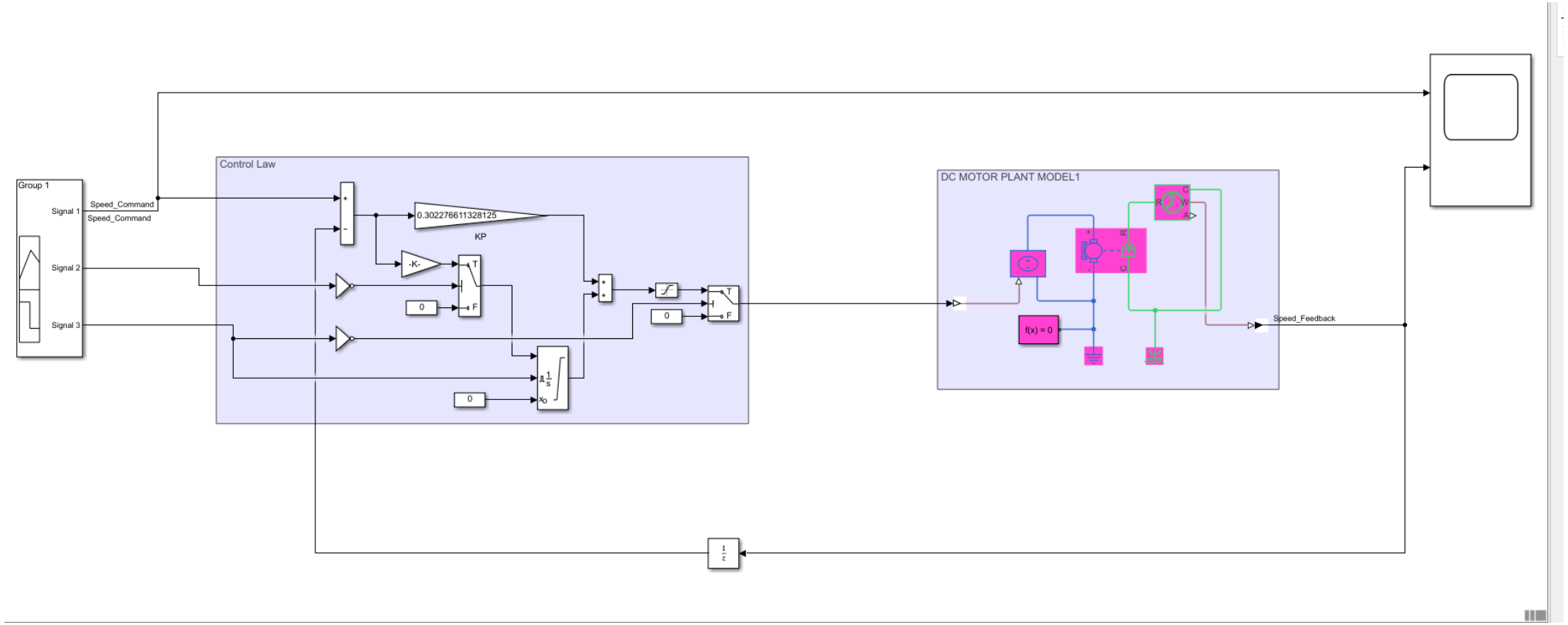
# SYSTEM MODEL FOR CONTROL LAW

- A simple PI control law with anti windup and command saturator in S domain



# SYSTEM MODEL FOR CONTROL LAW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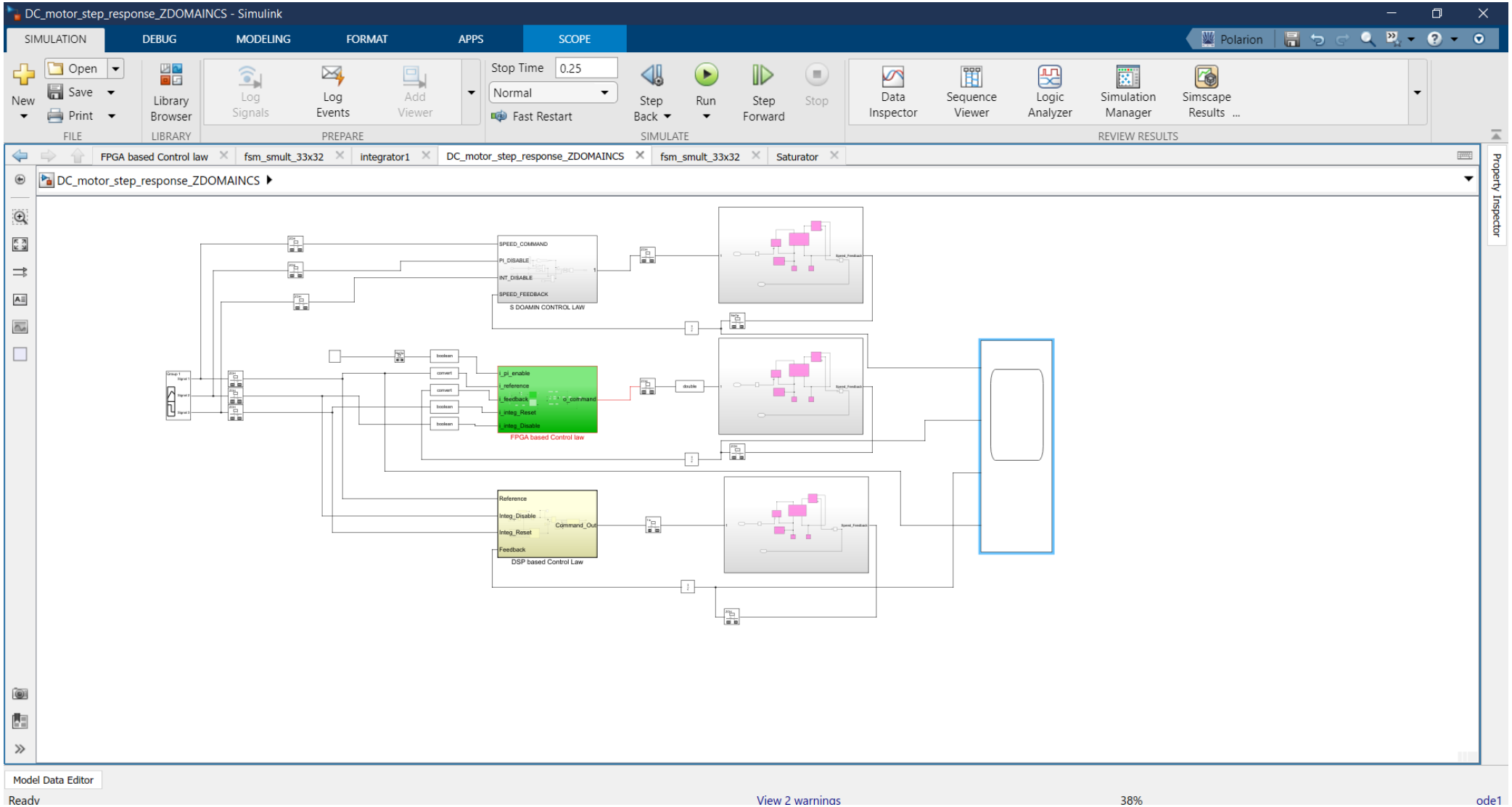
# CONTROL LAW IN DIFFERENT DOMAIN

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# MODEL IN LOOP FOR CONTROL LAW


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# MODEL IN LOOP FOR CONTROL LAW

## Post-Processing of results

| Step Response | S-domain Model | Floating Point Model (DSP) | Fixed point Model (FPGA) |
|---|---|---|---|
| RiseTime | 0.0125 | 0.0107 | 0.0121 |
| TransientTime | 0.0403 | 0.0374 | 0.0367 |
| SettlingTime | 0.0403 | 0.0374 | 0.0367 |
| SettlingMin | 361.0889 | 375.5305 | 366.0491 |
| SettlingMax | 416.3885 | 428.8628 | 414.4917 |
| Overshoot | 4.0971 | 7.2157 | 3.6229 |
| Undershoot | 0 | 0 | 0 |
| Peak | 416.3885 | 428.8628 | 414.4917 |
| PeakTime | 0.1475 | 0.144 | 0.146 |

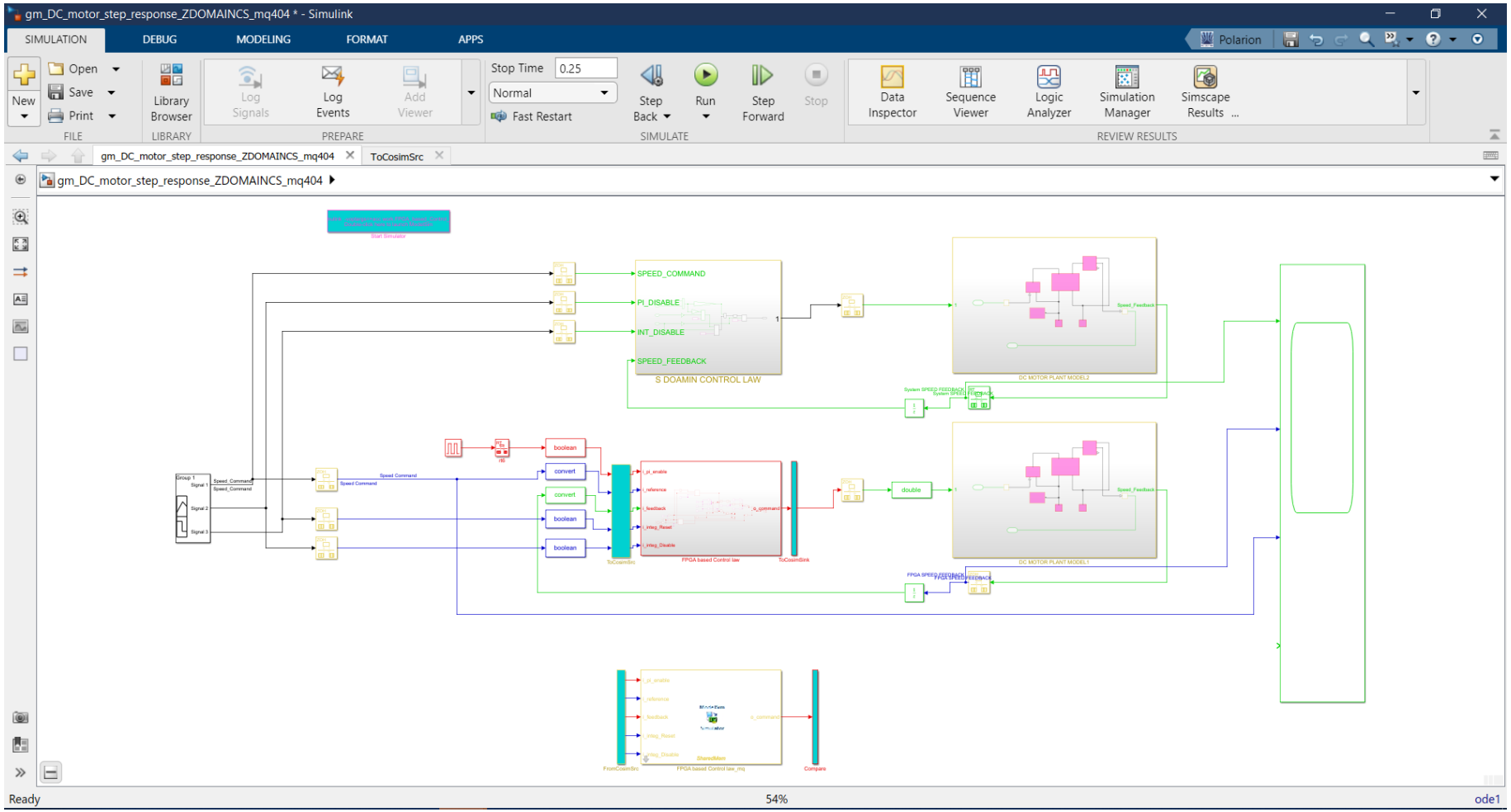
# HDL CO-SIMULATION

HDL co-simulation provide the following advantages:

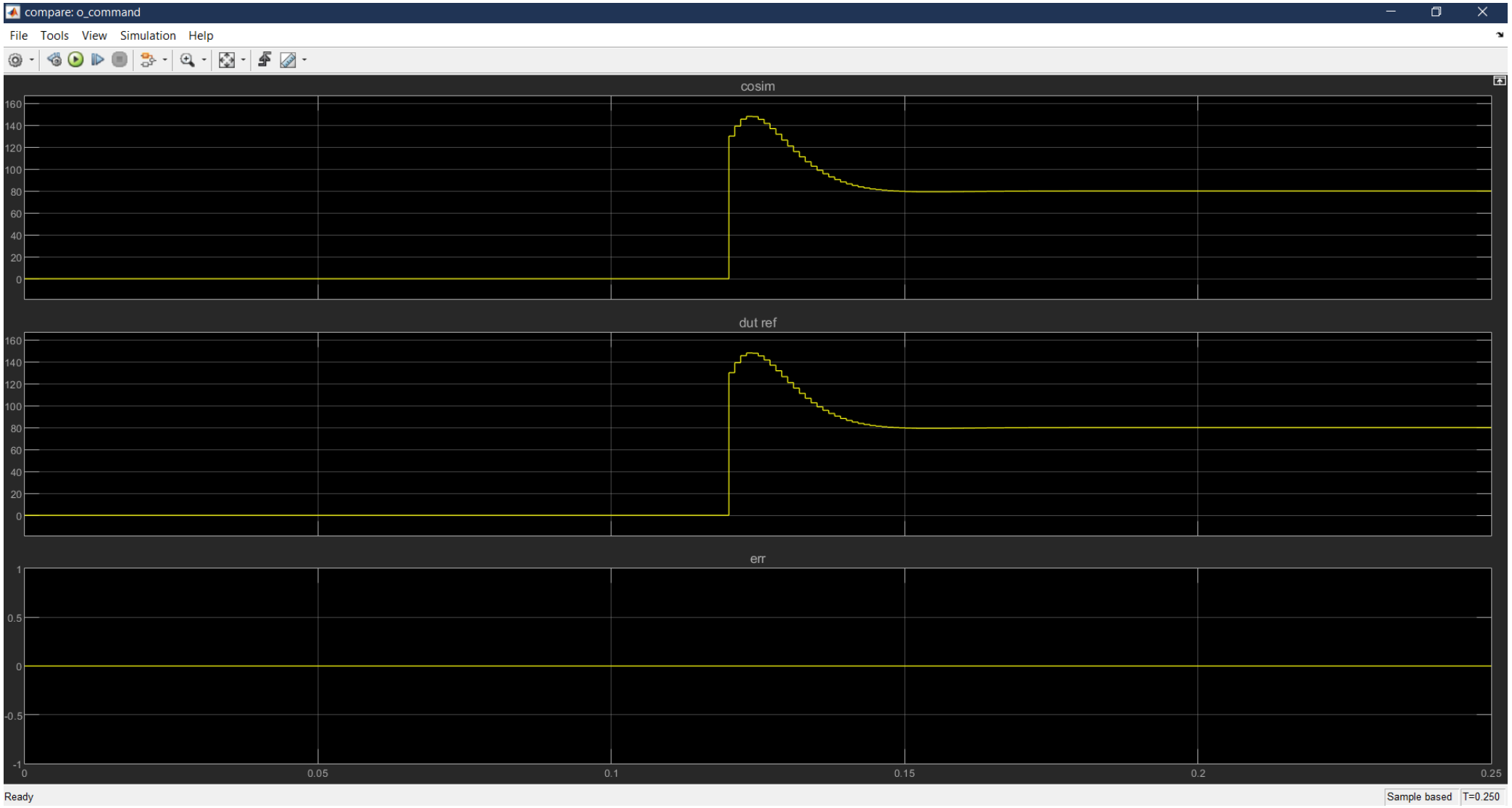
1. Design verification and validation
   - HDL code verification against its requirements (implementation correctness)
   - Validation of derived requirements such as sample time and discretization and fixed-point size

2. Virtual Integration
   - Muti-Domain simulation in one place to check the following:
     - Interface
     - Algorithm correctness
     - Dynamics of system

# CO-SIMULATION FOR CONTROL LAW (METHOD 1: AUTO GENERATED)



# CO-SIMULATION FOR CONTROL LAW

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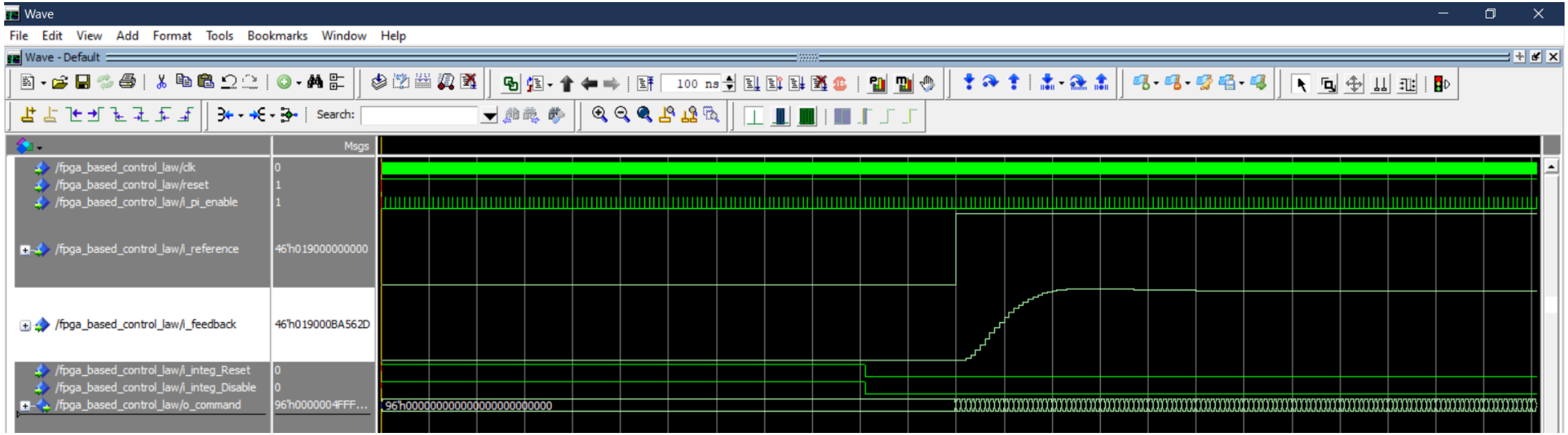
# CO-SIMULATION FOR CONTROL LAW

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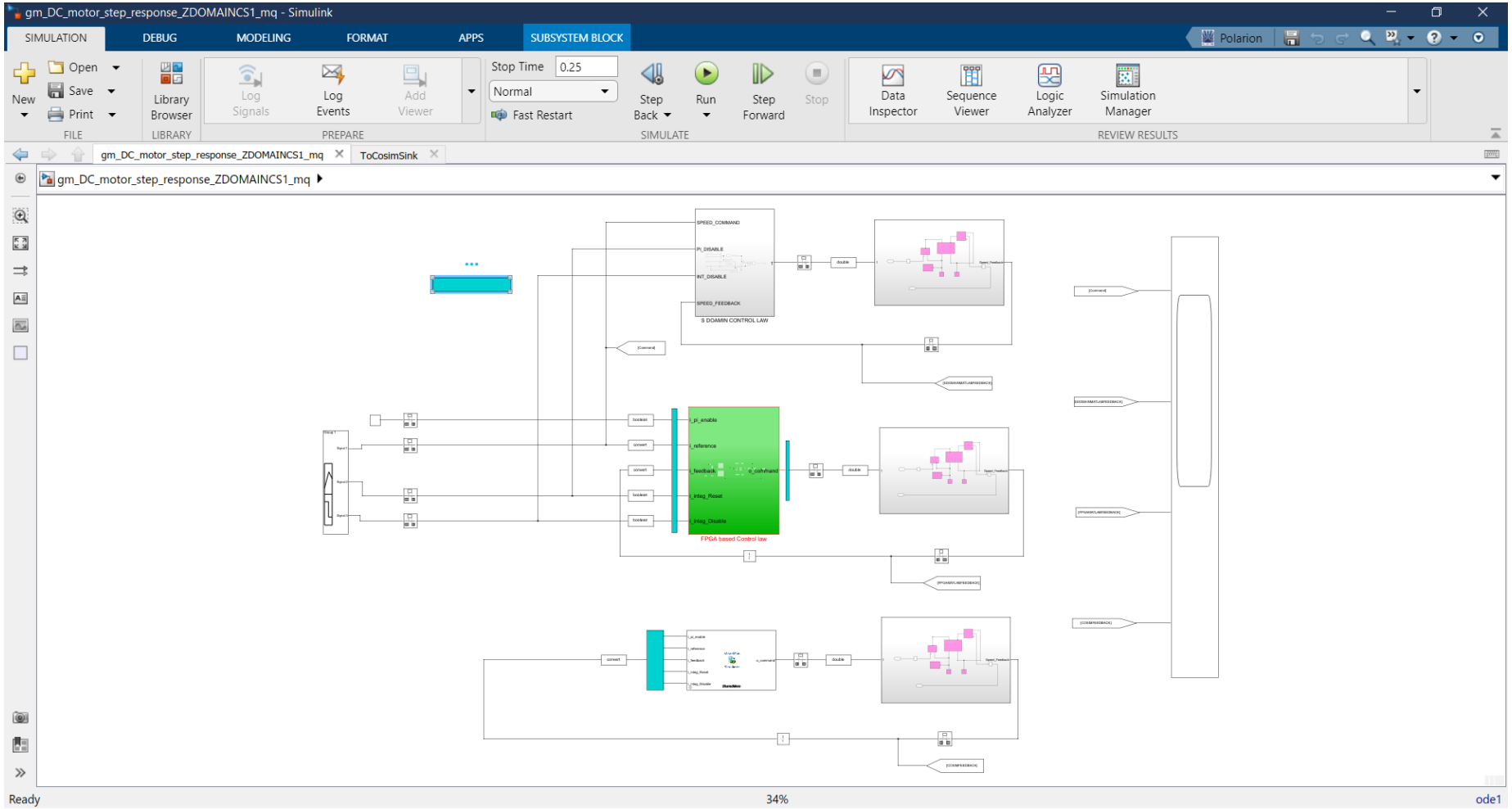
# CO-SIMULATION FOR CONTROL LAW (METHOD 2)

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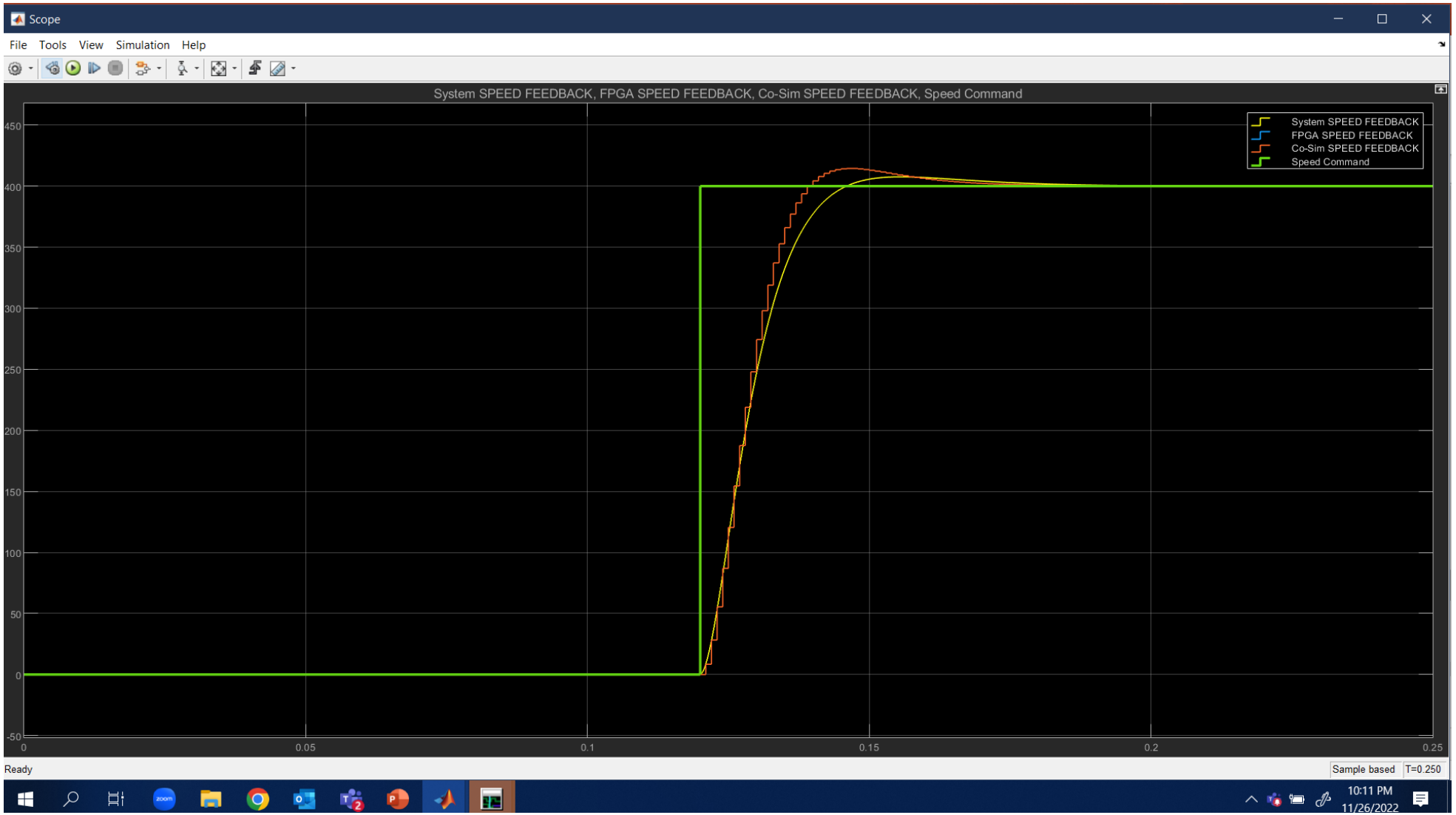
# CO-SIMULATION FOR CONTROL LAW

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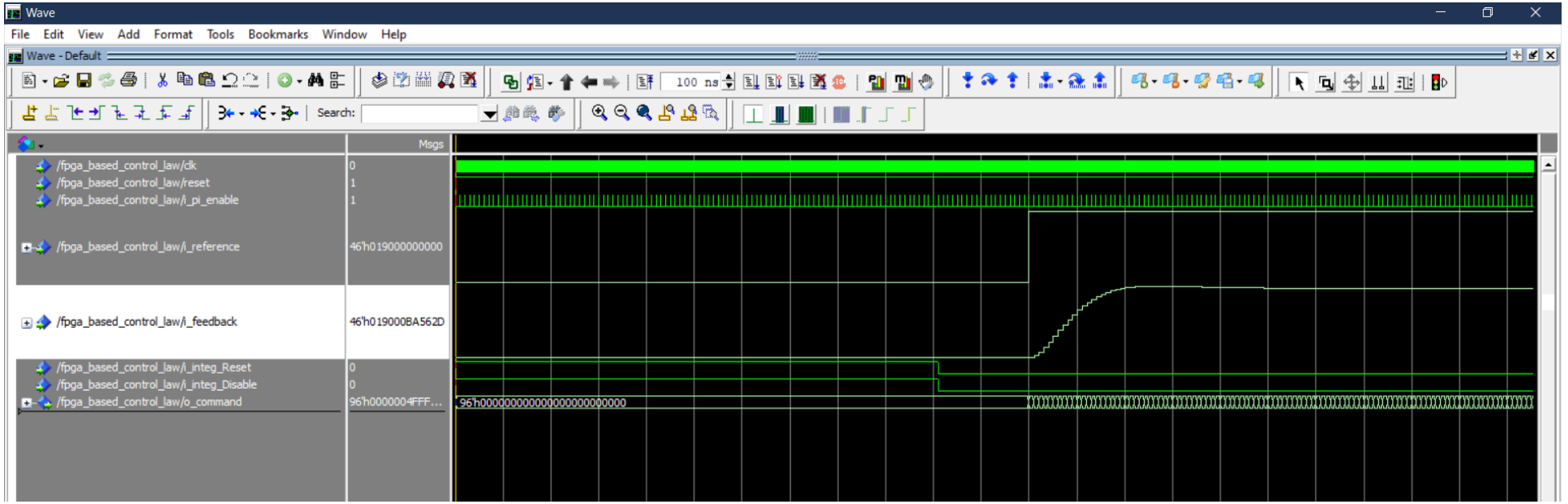
# CO-SIMULATION FOR CONTROL LAW




| Step Response | Fixed point Model (FPGA) Co-Simulation in QuestaSim | Fixed point Model (FPGA) Simulation in Mathwork |
|---|---|---|
| RiseTime | 0.0121 | 0.0121 |
| TransientTime | 0.0367 | 0.0367 |
| SettlingTime | 0.0367 | 0.0367 |
| SettlingMin | 366.0491 | 366.0491 |
| SettlingMax | 414.4917 | 414.4917 |
| Overshoot | 3.6229 | 3.6229 |
| Undershoot | 0 | 0 |
| Peak | 414.4917 | 414.4917 |
| PeakTime | 0.146 | 0.146 |

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# THANK YOU

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